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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/031,965	01/23/2002	Kentaro Hanma	WAT P-15/500727.20021	8635

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EXAMINER	
TANG, KUO LIANG J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/031,965	HANMA, KENTARO	
	Examiner	Art Unit	
	Kuo-Liang J Tang	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the application filed on 1/23/2002

The priority date for this application is 5/30/2001

Claims 1-15 are pending and have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8-11, 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al., US Patent No. 6,009,256 (hereinafter Tseng).

As Per Claim 1, Tseng teaches that the Simulation system provides four modes of operation: (1) Software Simulation, (2) Simulation via Hardware Acceleration, (3) In-Circuit Emulation (ICE), and (4) Post-Simulation Analysis. (E.g. see Abstract and associated text). In that Tseng discloses a system development support device, comprising:

"a division means (E.g. see FIG. 3, Simulation compiler 210 and associated text) for dividing a program, in which a logic specification of a system is described in a single high-level language (E.g. see FIG. 3, user circuit design as input data 200 and associated text), into a hardware portion (E.g. FIG. 3, reconfigurable hardware boards 250 and associated text) and a software portion (E.g. FIG. 3, code 215 and associated text) based on division information (E.g.

see col. 16:18-27, HDL file) which designates each portion of the program as either the hardware portion or the software portion";

"a storage means for storing a program of the hardware portion (E.g. see FIG. 3, reconfigurable hardware boards 250 and associated text, i.e. see col. 16:47-50) and a program of the software portion (E.g. see col. 16:39-43) which are divided by said division means";

"a first conversion means for converting the program of the hardware portion stored in said storage means into a circuit specification (E.g. see FIG. 3 and associated text, i.e. see col. 16: 28-38 and col. 16:51 – col. 17:7)"; and

"a second conversion means for converting the program of the software portion stored in said storage means into an execute form module specification (E.g. see FIG. 2-3 and associated text, i.e. see col. 11: 14-17)".

As Per claim 2, Tseng teaches:

"a division means (E.g. see FIG. 3, Simulation compiler 210 and associated text) for dividing a program, in which a logic specification of a system is described in a single high-level language (E.g. see FIG. 3, user circuit design as input data 200 and associated text), into a hardware portion (E.g. FIG. 3, reconfigurable hardware boards 250 and associated text) and a software portion (E.g. FIG. 3, code 215 and associated text) based on division information (E.g. see col. 16:18-27, HDL file) which designates each portion of the program as either the hardware portion or the software portion";

"a storage means for storing a program of the hardware portion (E.g. see FIG. 3, reconfigurable hardware boards 250 and associated text, i.e. see col. 16:47-50) and a program of the software portion (E.g. see col. 16:39-43) which are divided by said division means";

"a first conversion means for converting the program of the hardware portion stored in said storage means into a circuit specification (E.g. see FIG. 3 and associated text, i.e. see col. 16: 28-38 and col. 16:51 – col. 17:7)"; and

"a second conversion means for converting the program of the software portion stored in said storage means into an execute form module specification (E.g. see FIG. 2-3 and associated text, i.e. see col. 11: 14-17)";

"said division means determining, in each function block (E.g. see col. 16:28-38, component) of the program described in the single high-level language (E.g. see col. 16:28-38, HDL), whether the function block is a portion to be mounted as hardware or a portion to be mounted as software based on the division information (E.g. see col. 16:28-38)".

As Per claim 3, the rejection of claim 1 is incorporated and further Tseng teaches: "a division information generating means for generating the division information based on a specification of the system (E.g. see FIG. 3, Simulation compiler 210 and associated text)".

As Per claim 4, the rejection of claim 1 is incorporated and further Tseng teaches: "a division information generating means for generating the division information based on capacity of a memory in which the execute form module is stored in the system (E.g. see col. 16:39-43) and number of gates of a gate array in which a circuit based on the circuit specification

is performed in the system (E.g. see FIG. 3, reconfigurable hardware boards 250 and associated text, i.e. see col. 16:47-50) or ...".

As Per claim 5, the rejection of claim 1 is incorporated and further Tseng teaches:

"a verification means for verifying a circuit based on the circuit specification resulting from the conversion by said first conversion means and an operation of the execute form module resulting from the conversion by said second conversion means (E.g. see col. 1:7-11)".

As Per claim 6, the rejection of claim 5 is incorporated and further Tseng teaches:

"a division information changing means for changing the division information in accordance with a result of verification by said verification means (E.g. see col. 13:44-47)".

As Per claim 8, the rejection of claim 5 is incorporated and further Tseng teaches:

"a first condition changing means for changing a hardware condition which said first conversion means refers to when converting the hardware portion into the circuit specification in accordance with a result of verification by said verification means (E.g. see col. 13:44-47)".

As Per claim 9, the rejection of claim 5 is incorporated and further Tseng teaches:

"a first condition changing means for changing a hardware condition which said first conversion means refers to when converting the hardware portion into the circuit specification in accordance with a result of verification by said verification means (E.g. see col. 13:44-47), said

first condition changing means changing input/output timing of signals (E.g. see col. 20:25-38) between the hardware portion and the software portion in accordance with the result of the verification by said verification means".

As Per claim 10, the rejection of claim 5 is incorporated and further Tseng teaches:

"a second condition changing means for changing a compile condition on which said second conversion means converts the program of the software portion into the execute form module in accordance with a result of verification by said verification means (E.g. see col. 3:40 – col. 4:14) ".

As Per claim 11, the rejection of claim 5 is incorporated and further Tseng teaches:

"a second condition changing means for changing a compile condition when said second conversion means converts the program of the software portion into the execute form module in accordance with a result of verification by said verification means, said second condition changing means changing a type of a CPU core used in the system in accordance with the result of the verification by said verification means (E.g. see col. 11:1-17)".

As Per claim 13, Tseng teaches a system development support method, comprising the steps of :

"dividing a program (E.g. see FIG. 3, Simulation compiler 210 and associated text), in which a logic specification of a system is described in a single high-level language (E.g. see FIG. 3, user circuit design as input data 200 and associated text), into a hardware portion (E.g. FIG. 3,

reconfigurable hardware boards 250 and associated text) and a software portion (E.g. FIG. 3, code 215 and associated text) based on division information which designates each portion of the program as either the hardware portion or the software portion (E.g. see FIG. 3 and associated text)";

"converting a program of the hardware portion into a circuit specification (E.g. see FIG. 3 and associated text, i.e. see col. 16: 28-38 and col. 16:51 – col. 17:7)"; and

"converting a program of the software portion into an execute form module (E.g. see FIG. 2-3 and associated text, i.e. see col. 11: 14-17)".

As Per Claim 14, is the computer-readable record medium claim corresponding to the system claim 13 and is rejected under the same reason set forth in connection of the rejection of claim 13.

As Per Claim 15, is the computer-readable record medium claim corresponding to the subset of system claim 13 and is rejected under the same reason set forth in connection of the rejection of claim 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Klein et al. US Patent No. 6,212,489 (hereinafter Klein).

As Per claim 7, the rejection of claim 5 is incorporated and further Tseng doesn't explicitly disclose changing a ratio of the hardware portion to the software portion in accordance with a result of verification by said verification means. However, Klein in an analogous art teaches in a manner such as changing a ratio of the hardware portion to the software portion in accordance with a result of verification by said verification means (see ABSTRACT and col. 3:17-28). Therefore, it would have been obvious to incorporate the teaching of Tseng into the teaching of Klein to change a ratio of the hardware portion to the software portion in accordance with a result of verification by said verification means. The modification would have been obvious because one of ordinary skill in the art would have been motivated to optimize a hardware-software co-verification system.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng in view of Killian et al. US Patent No. 6,477,683 (hereinafter Killian).

As Per claim 12, the rejection of claim 5 is incorporated and further Tseng doesn't explicitly disclose an optimization means for repeatedly operating said division means. However, Killian in an analogous art teaches in a manner such as an optimization means for repeatedly operating said division means, said first conversion means, said second conversion means and said verification means while changing at least one of the division information,

hardware conditions on which said first conversion means converts the program of the hardware portion into the circuit specification, compile conditions on which said second conversion means converts the program of the software portion into the execute form module, until a predetermined verification result is obtained or only a predetermined number of repetitions (see Col. 35:29-43). Therefore, it would have been obvious to incorporate the teaching of Tseng into the teaching of Killian to have an optimization means for repeatedly operating said division means. The modification would have been obvious because one of ordinary skill in the art would have been motivated to improve system performance and cost.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuo-Liang J Tang whose telephone number is 703-305-4866. The examiner can normally be reached on 8:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 703-305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

After October 25, 2004, examiner can be reached at new telephone number (571) 272-3705, and the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kuo-Liang J. Tang

Software Engineer Patent Examiner

TUAN DAM
SUPERVISORY PATENT EXAMINER